KARTHIKEYA KOLLU

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OBJECTIVE

I intend to establish myself as a dedicated and accomplished VLSI professional, actively seeking opportunities in the field of VLSI. I am committed to contributing to the growth of the organisation and, in turn, fostering my personal and professional development within the company.

EDUCATION

Bachelor of Technology in Electronics and Communication Engineering,
Rajiv Gandhi University of Knowledge Technologies, Ongole campus, Andhra Pradesh, India 2019 - 2023
CGPA : 9.35

Pre-University Course ,
Rajiv Gandhi University of Knowledge Technologies, Ongole campus, Andhra Pradesh, India 2017 - 2019
CGPA : 9.42

Class 10th ,
VMC High School, Vijayawada, Andhra Pradesh, India 2016 - 2017
CGPA : 10.0

SKILLS

Technical Skills	ASIC Design, RTL coding, Computer Organization and Architecture, CMOS Fundamentals, Scripting, Digtal Logic Design, FPGA RTL Coding
Soft Skills	Team Work, Communication Skills, Time Management, Problem Solving
HDL Languages	Verilog, System Verilog
Programming Languages	Python, C, C++, TCL/TK, Bash shell, GNU makefile
Communication Languages	English, Hindi, Telugu
Tools	LTspice, Mentor Questa, Synopsys VCS, Cadence Xcelium
Protocols	Off chip protocols : I2C, UART, SPI On-Chip protocols : APB, AHB

PROJECTS

RISC-V Processor RTL Design and Functional Verification

Project Overview **:**

Designed and implemented the RTL code for a RISC-V based processor, ensuring compliance with RISC-V ISA specifications. Developeded System Verilog test-bench for the design.

Responsibilities**:**

1. Designed and Implemented RTL Code for a RISC-V based processor.
2. Developed System Verilog testbenches to verify the functionality of the processor.

Key Achievements**:**

1. Successfully completed the RTL design and verification, ensuring adherence to RISC-V architecture specifications.
2. Identified and resolved critical bugs through rigorous testing and debugging.

Technologies Used**:**

System Verilog, RISC-V ISA, Verilog ***Github Link:*** —— https://github.com/alpha-karthik/RISCV

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AHB to APB Bridge RTL Implementation and Verification

***Project Overview* :**

Led the complete design and RTL implementation of an AHB (Advanced High-Performance Bus) to APB (Advanced Peripheral Bus) Bridge, a crucial interface enabling communication between different bus architectures. Conducted in-depth functional verification using System Verilog test-benches to ensure protocol adherence and robustness.

***Responsibilities*:**

1. Designed and implemented the RTL code for the AHB to APB Bridge, considering protocol specifications and inter-bus communication requirements.

2.Developed and executed System Verilog test-benches for functional verification, thoroughly validating the bridge's operation.

***Key Achievements*:**

1. Successfully delivered a fully functional AHB to APB Bridge RTL design, meeting project milestones and requirements.

2. Conducted extensive testing, identifying and resolving critical issues to ensure seamless bus communication.

3. Validated the AHB to APB Bridge's functionality using Verification techniques, resulting in a highly reliable and robust design.

***Technolgies Used*:**

System Verilog, RTL, AHB, APB, Bus Protocols ***Github Link:*** https://github.com/alpha-karthik/AHB-APB-Bridge

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UART Protocol RTL Design and Functional Verification

***Project Overview* :**

Developed and implemented the RTL code for a UART (Universal Asynchronous Receiver/Transmitter) Protocol, a crucial component for serial communication in digital systems. Conducted functional verification using System Verilog test-benches to ensure protocol compliance and reliability.

***Responsibilities*:**

1. Designed and coded the RTL implementation of the UART Protocol.

2. Created System Verilog test-benches for functional verification of the UART Protocol.

***Key Achievements*:**

1. Successfully completed the RTL design, meeting UART protocol specifications.

2. Conducted thorough testing, identifying and fixing critical issues to ensure protocol accuracy.

***Technologies Used*:**

System Verilog, UART Protocol, Verilog ***Github Link:*** —— https://github.com/alpha-karthik/UART

EXPERIENCE INTERNSHIP

- Completed an internship with Emertxe Technologies in IoT Domain. jun 2022 - sep 2022

DECLARATION

- I hereby declare that the above-mentioned information is true and correct to the best of my knowledge and belief. I understand that any false statement or omission of facts may result in disqualification from consideration for employment or termination if already employed.

K.Karthikeya